36. (NEW) The method of Claim 35, wherein at least the steps of storing the first datum, precharging bitlines and storing the second datum are completed within one access cycle of the memory structure.

37. (NEW) The method of Claim 34, wherein the first memory structure location is the same as the second memory structure location.

38. (NEW) A single-port memory structure having a predetermined memory access speed and a memory access period, comprising:

(a) memory cells disposed to store data;

(b) global row decoders of selected ones of the memory cells; and

(c) a predecoding circuit coupled with selected global row decoders, wherein the predecoding circuit is disposed to provide predecoding at a speed substantially faster than the predetermined memory structure access speed, and allowing access to a selected memory cell at least twice during the memory access period, thereby providing dual-port functionality thereby.

39. (NEW) The single-port memory structure of Claim 38, wherein the predecoding circuit is disposed to provide predecoding at a speed more than twice the predetermined memory structure access speed, and allowing access to a selected memory cell three or more times during the memory access period, thereby providing multi-port functionality thereby.

REMARKS

Claims 1-22 have been cancelled and new claims 23-39 have been substituted.

The amendments to the specification are the same amendments allowed in the parent application.

A Notice of Allowability respecting all pending claims 23-39 is courteously solicited.

Please charge any underpayment of fees required by this submission to the deposit account of McAndrews, Held & Malloy, Ltd., Account No. 13-0017.

Respectfully submitted,

Dated: July 2, 2003

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